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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,713	05/16/2001	Jen-Kai Chen	SUND 202	9412

23995 7590 11/03/2004

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EXAMINER	
DAVIS, CYNTHIA L	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,713	CHEN ET AL.	
	Examiner	Art Unit	
	Cynthia L Davis	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 May 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 9-14, and 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte in view of Yoshida.

Regarding claim 1, reading the M-th QLN corresponding to the M-th packet for obtaining an inter-packet gap, and then transmitting the M-th packets, triggering the second counter, stopping the second counter when a counted value by the second counter is equal to a clock cycle value corresponding to the inter-packet gap, reading the QLN of the (M+1)-th packet, transmitting the M-th packet, and increasing M by 1 are disclosed in Kalkunte, in figure 3A, and column 6, lines 26-31 (this process is repeated for every packet in the switch). Claim 1 further specifies a receive process, which is missing from Kalkunte. However, receiving the N-th packet, triggering the first counter, performing a counting operation by the first counter, and stopping the first counter when the (N+1)-th packet arrives, then recording an inter-packet gap between the N-th packet and the (N+1)-th packet according to a counting value by the first counter, increasing N

by 1 and repeating is disclosed in column 6, lines 61-64 of Yoshida. It would have been obvious to one skilled in the art at the time of the invention to use the receive process of Yoshida in conjunction with the transmit process of Kalkunte. The motivation would be to obtain an optimum transmission time for each packet. Also, claim 1 specifies QLN's that hold information corresponding to each packet, which is missing from Kalkunte. However, Kalkunte has access to all the information that the process of the instant application would store in the QLN with regards to each packet. It would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN. The motivation would be to have all the information for each packet.

Regarding claim 9, reading the M-th QLN corresponding to the M-th packet for obtaining an inter-packet gap, and then transmitting the M-th packets, triggering the second counter, stopping the second counter when a counted value by the second counter is equal to a clock cycle value corresponding to the inter-packet gap, reading the QLN of the (M+1)-th packet, transmitting the M-th packet, and increasing M by 1 are disclosed in Kalkunte, in figure 3A, and column 6, lines 26-31 (this process is repeated for every packet in the switch). Claim 9 further specifies a receive process, which is missing from Kalkunte. However, receiving the N-th packet, triggering the first counter, performing a counting operation by the first counter, and stopping the first counter when the (N+1)-th packet arrives, then recording an inter-packet gap between the N-th packet and the (N+1)-th packet according to a counting value by the first counter, increasing N by 1 and repeating is disclosed in column 6, lines 61-64 of Yoshida. It would have

been obvious to one skilled in the art at the time of the invention to use the receive process of Yoshida in conjunction with the transmit process of Kalkunte. The motivation would be to obtain an optimum transmission time for each packet. A TMAC unit is disclosed in Kalkunte, figure 6, element 22. Claim 9 further specifies the switch further comprising an RMAC, which is missing from Kalkunte. While this is not specifically disclosed in Yoshida, a switch that receives packets is disclosed in figure 7. It would have been obvious to one skilled in the art at the time of the invention to include a RMAC in the switch. The motivation would be to have a unit to process the receiving of packets. Claim 9 also specifies 2 counters. One is disclosed in figure 6, element 604 of Kalkunte. The second is missing from Kalkunte. While it is not specifically disclosed in Yoshida, a counter that processes the receipt of packets is disclosed in column 6, lines 61-64. It would have been obvious to one skilled in the art at the time of the invention to have a second counter. The motivation would be to be able to count the receive times. Lastly, claim 9 specifies QLN's that hold information corresponding to each packet, which is missing from Kalkunte. However, Kalkunte has access to all the information that the process of the instant application would store in the QLN with regards to each packet. It would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN. The motivation would be to have all the information for each packet.

Regarding claim 16, one counter is disclosed in figure 6, element 604 of Kalkunte. The second is missing from Kalkunte. While it is not specifically disclosed in Yoshida, a counter that processes the receipt of packets is disclosed in column 6, lines

61-64. It would have been obvious to one skilled in the art at the time of the invention to have a second counter. The motivation would be to be able to count the receive times. A TMAC unit is disclosed in Kalkunte, figure 6, element 22. Claim 16 further specifies the switch further comprising an RMAC, which is missing from Kalkunte. While this is not specifically disclosed in Yoshida, a switch that receives packets is disclosed in figure 7. It would have been obvious to one skilled in the art at the time of the invention to include a RMAC in the switch. The motivation would be to have a unit to process the receiving of packets. Claim 16 also specifies QLN's that hold information corresponding to each packet, which is missing from Kalkunte. However, Kalkunte has access to all the information that the process of the instant application would store in the QLN with regards to each packet. It would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN. The motivation would be to have all the information for each packet. The TMAC being used for reading the M-th QLN to obtain an IPG and then transmitting the M-th packet, then triggering the second counter, wherein when a counted value by the second counter is equal to a clock cycle value corresponding to the IPG, reading the next packet's IPG and transmitting next packet is disclosed in Kalkunte, in figure 3A, and column 6, lines 26-31 (this process is repeated for every packet in the switch). Lastly, claim 16 specifies that the RMAC is used for triggering the first counter to obtain an IPG between the N-th packet and the (N+1)-th packet, then recording the IPG, which is missing from Kalkunte. This is disclosed in column 6, lines 61-64 of Yoshida. It would have been obvious to one skilled in the art at the time of the invention to use the receive process of Yoshida in

conjunction with the transmit process of Kalkunte. The motivation would be to obtain an optimum transmission time for each packet.

Regarding claim 2, a TMAC unit is disclosed in Kalkunte, figure 6, element 22. Claim 2 further specifies the switch further comprising an RMAC, which is missing from Kalkunte. While this is not specifically disclosed in Yoshida, a switch that receives packets is disclosed in figure 7. It would have been obvious to one skilled in the art at the time of the invention to include a RMAC in the switch. The motivation would be to have a unit to process the receiving of packets.

Regarding claims 3, 10, and 17, the second counter being in the TMAC is disclosed in figure 6, element 604 of Kalkunte. Claims 3, 10 and 17 further specify the first counter being in the RMAC unit, which is missing from Kalkunte. While this is not specifically disclosed in Yoshida, a counter that processes the receipt of packets is disclosed in column 6, lines 61-64. It would have been obvious to one skilled in the art at the time of the invention to put the first counter in the RMAC. The motivation would be to put the counter with the unit that receives the packets that the counter must process.

Regarding claims 4, 12, and 18, a first field for recording a memory address for temporally storing the next packet is disclosed in column 4, line 63 (the FIFO buffer contains the packet, and necessarily, its address). A second field for recording a destination port of the N-th packet is disclosed in figure 7 of Kalkunte (destination address field). A third field for recording a size of the N-th packet is disclosed in column 7, lines 45-46 and figure 7 of Kalkunte (length field). A fourth field for recording an inter-

packet gap is disclosed in column 7, lines 17-19. Claims 4, 12, and 18 further specify all this information being stored together in a QLN, which is not specifically disclosed in Kalkunte. However, Kalkunte does have access to all of this information, and can associate it with each packet. It would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN. The motivation would be to have all the information for each packet.

Regarding claims 5, 7, 14, 20, 21, and 22, a fifth field in the QLN for recording a source port speed of the N-th packet is not specifically disclosed in Kalkunte. However, Kalkunte does disclose each station receiving from the network manager a desired transmission rate that is based on the speeds of all of the stations in column 5, lines 20-32, and column 6, lines 6-10. It would have been obvious to one skilled in the art at the time of the invention to store the source port speed. The motivation would be to have more information about the network to use in optimizing transmission times.

Regarding claims 6, 13, and 19, a first field for recording a memory address for temporarily storing the (N+1)-th packet is disclosed in column 4, line 63 (the FIFO buffer contains the packet, and necessarily, its address). A second field for recording a destination port of the N-th packet is disclosed in figure 7 of Kalkunte (destination address field). A third field for recording the size of the N-th packet in column 7, lines 45-46 and figure 7 of Kalkunte (length field). Claims 6, 13, and 19 further specify a fourth field for recording a clock cycle value corresponding to 96 bit time minus the inter-packet gap, which is not specifically disclosed in Kalkunte. However, Kalkunte does disclosed in column 7, lines 17-19 storing the inter-packet gap. Yoshida discloses in

column 4, lines 38-42, making a comparison between the expected inter-packet gap and the actual inter-packet gap. It would have been obvious to one skilled in the art at the time of the invention to store the inter-packet gap the format of 96 bit time minus the inter-packet gap. The motivation would be to store the actual inter-packet gap's amount of offset from the expected inter-packet gap. Claims 6, 13, and 19 also further specify all this information being stored together in a QLN, which is not specifically disclosed in Kalkunte. However, Kalkunte does have access to all of this information, and can associate it with each packet. It would have been obvious to one skilled in the art at the time of the invention to put all of this information in a QLN. The motivation would be to have all the information for each packet.

Regarding claim 11, the packets inputted to the switch being temporarily stored in memory is disclosed in Kalkunte, column 4, line 63 (the FIFO buffer contains the packet).

3. Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte in view of Yoshida in further view of Sanderson. The peripheral device being a test device is missing from Kalkunte and Yoshida. However, Sanderson discloses in figure 1 a test device connected to a switch. It would have been obvious to one skilled in the art at the time of the invention to use a test device. The motivation would be to gain diagnostic information about the switch.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia L Davis whose telephone number is (571) 272-3117. The examiner can normally be reached on 8:30 to 6, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLD
10/8/2004 CLD 10/8/04

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